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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,932	10/09/2003	Kenneth R. Schulz	1934-15-3	2201

7590 02/13/2006

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EXAMINER	
ZALEPA, GEORGE D	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/683,932	SCHULZ ET AL.	
	Examiner	Art Unit	
	George D. Zalepa	2183	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file:

a. Information Disclosure Statements as filed on 11 April 2005 and 19 September 2005

b. Declaration as filed on 9 October 2003.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Pipeline accelerator consisting of multiple hard-wired pipeline circuits interacting via communication and pipeline busses.

4. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: In paragraph 10, specification refers to "coprocessor 24_n" where element 24_n in the drawings is labeled as a memory unit. Furthermore, in numerous paragraphs, applicant uses the phrase "Serial No(s). ___". Applicant is requested to insert serial number of related patent application in place of underscores.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-7, 9-13, 15-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong et al (US Pat. No. 6,282,627; herein referred to as "Wong").

7. Regarding **independent claim 1,**

8. Wong discloses *a pipeline accelerator, comprising: a communication bus* [see Wong, Fig. 6, element 609; Col. 5, lines 24-26]*; and a plurality of pipeline units each coupled to the communication bus* [see Wong, Fig. 3, element "Datapath Slice"; Col. 5, lines 30-34] *and each comprising a respective hardwired-pipeline circuit* [see Wong, Fig. 6, elements "DPU"; Col. 5, lines 12-15 ("The DPUs provide the data path functionality for the behavioral mapping…")].

9. Regarding **claim 2,**

10. Wong discloses *the pipeline accelerator of claim 1 wherein each of the pipeline units comprises: a respective memory coupled to the hardwired-pipeline circuit* [see Wong, Fig. 7, element LSM; Col. 4, lines 28-31]*; and wherein the hardwired-pipeline circuit is operable to, receive data from the communication bus* [see Wong, Fig. 6/7, element 609; Col. 5, lines 24-26]*, load the data into the memory* [see Wong, Col. 9, lines 2-4 ("loading coprocessor registers")]*, retrieve the data from the memory* [see Wong, Col. 4, lines 55-57; Examiner's note: Wong discloses data passing from a register (within the ACM/LSM fabric) to a DPU ("cloud"), thus Wong discloses reading data from a memory coupled to a hardwire-pipeline circuit.]*, process the retrieved data* [see Wong, Fig. 5, element 503; Examiner's note: Wong discloses a "cloud" of reconfigurable logic which processes data sent from the previously cited

register.], *and drive the processed data onto the communication bus* [see Wong, Col. 9, lines 4-7; Examiner's note: Wong discloses results being sent back to the main processor, which would have utilized the communication bus.].

11. Regarding **claim 3**,

12. Wong discloses *the pipeline accelerator of claim 1 wherein each of the pipeline units comprises: a respective memory coupled to the hardwired-pipeline circuit* [see Wong, Fig. 7, element LSM]; *and wherein the hardwired-pipeline circuit is operable to, receive data from the communication bus* [see Wong, Fig. 6/7, element 609; Col. 5, lines 24-26], *process the data* [see Wong, Fig. 5, element 503; Examiner's note: Wong discloses a "cloud" of reconfigurable logic which processes data sent from the previously cited register.], *load the processed data into the memory* [see Wong, Col. 4, lines 55-57; Examiner's note: In the cited sections, Wong discloses a circular movement of data, however it is apparent upon reading the specification that the flow of data is not necessarily in a circular motion (Col. 9, lines 47-50). This allows a serial connection of datapath elements such as combinational logic to a register and then returned to processor. Due to the reconfigurable nature of the ACM it is impractical to list or summarize all possible function configurations, therefore, the previously described configuration is considered to be of merit by the examiner.], *retrieve the processed data from the memory, and load the processed data onto the communication bus* [see Wong, Col. 9, lines 4-7; Examiner's note: Wong discloses results being sent back to the main processor, which would have utilized the communication bus and would also retrieve the values from a stored location within the ACM.].

13. Regarding **claim 5**,

14. Wong discloses *the pipeline accelerator of claim 1, further comprising: a pipeline bus* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24; Examiner's note: It would have been obvious to one of ordinary skill in the art at the time of invention that the bus interfaces would have been coupled to the

CPU and to a corresponding datapath slice though a bus.]; *and a pipeline-bus interface coupled to the communication bus and to the pipeline bus* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24].

15. Regarding **claim 6,**

16. Wong discloses *the pipeline accelerator of claim 1, further comprising: wherein the communication bus comprises a plurality of branches* [see Wong, Fig. 6, double-arrowed busses between communication bus **609** and elements **610a,b**], *a respective branch coupled to each pipeline unit* [see Wong, Fig. 6, coupling of double sided arrow to 610a/620a]; *and a router coupled to each of the branches* [see Wong, Fig. 6, element 611a,b; Examiner's note: elements 611a/b determine the interconnect if any between DPUs (Col. 5, lines 26-28) thus routing functions to individual pipeline units.].

17. Regarding **claim 7,**

18. Wong discloses *the pipeline accelerator of claim 1, further comprising: wherein the communication bus comprises a plurality of branches* [see Wong, Fig. 6, double-arrowed busses between communication bus 609 and elements 610a,b], *a respective branch* [see Wong, Fig. 6, double-arrowed busses between communication bus 609 and elements 610a,b] *coupled to each pipeline unit* [see Wong, Fig. 6, element 610a,b]; *a router coupled to each of the branches* [s see Wong, Fig. 6, element 611a,b; Examiner's note: elements 611a/b determine the interconnect if any between DPUs (Col. 5, lines 26-28) thus routing functions to individual pipeline units.]; *a pipeline bus* [see Wong, Fig. 3, elements 319a,b; Examiner's note: It would have been obvious to one of ordinary skill in the art at the time of invention that the bus interfaces would have been coupled to the CPU and to a corresponding datapath slice via a bus]; *and a pipeline-bus interface coupled to the router and to the pipeline bus* [see Wong, Fig. 3, elements 319a,b].

19. Regarding **claim 9,**

20. Wong discloses *the pipeline accelerator of claim 1 wherein: the communication bus is operable to receive data addressed to one of the pipeline units* [see Wong, Col. 9, lines 2-4]*; and the one pipeline circuit is operable to accept the data; and the other pipeline circuits are operable to reject the data* [see Wong, Col. 10, lines 7-10; lines 37-45; Examiner's note: Wong uses the function map table (Fig. 18a) to and the block configuration words (Fig. 18b) to correctly allow the corresponding pipeline unit to process the data and the other pipeline units to reject processing of the data.].

21. Regarding **claim 10**,

22. Wong discloses *the pipeline accelerator of claim 1, further comprising: wherein the communication bus comprises a plurality of branches* [see Wong, Fig. 6, double-arrowed busses between communication bus **609** and elements **610a,b**]*, a respective branch coupled to each pipeline unit* [see Wong, Fig. 6, coupling of double sided arrow to 610a/620a]*; a router coupled to each of the branches* [see Wong, Fig. 6, element 611a,b; Examiner's note: elements 611a/b determine the interconnect if any between DPUs (Col. 5, lines 26-28)] *and operable to, receive data addressed to one of the pipeline units* [see Wong, Col. 9, lines 2-4; Examiner's note: Applicant is reminded of the method disclosed by Wong to identify a receiving pipeline unit as describe with regard to claim 9 of this application.]*, and provide the data to the one pipeline unit via the respective branch of the communication bus* [Examiner's note: It is clear that data sent to a particular pipeline would be required to utilize the branch bus disclosed by Wong in Fig. 6, double-arrowed busses between communication bus 609 and elements 610a,b].

23. Regarding **independent claim 11**,

24. Wong discloses *a computing machine, comprising: a processor* [see Wong, Fig. 3, element 302]*; a pipeline bus coupled to the processor* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24; Examiner's note: It would have been obvious to one of ordinary skill in the art at the time of invention that the bus interfaces would have been coupled to the CPU and to a corresponding datapath slice via a bus]*; and a pipeline accelerator comprising, a communication bus* [see Wong, Fig. 6, element 609; Col.

5, lines 24-26], *a pipeline-bus interface coupled between the pipeline bus and the communication bus* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24], *and a plurality of pipeline units each coupled to the communication bus* [see Wong, Fig. 3, element "Datapath Slice"; Col. 5, lines 30-34] *and each comprising a respective hardwired-pipeline circuit* [see Wong, Fig. 6, elements "DPU"; Col. 5, lines 12-15 ("The DPUs provide the data path functionality for the behavioral mapping...")].

25. Regarding **claim 12,**

26. Wong discloses *the computing machine of clam 11 wherein: the processor is operable to generate a message that identifies one of the pipeline units* [see Wong, Col. 9, lines 2-4 (instruction to turn control over to ACM); Col. 10, line 37 (a load instruction to specify which plane of DPUs to load)] *and to drive the message onto the pipeline bus* [Examiner's note: It is inherent with respect to Figure 3, that data is transferred between the CPU and ACM via a bus and bus interfaces]*; the pipeline-bus interface is operable to couple the message to the communication bus* [see Wong, Fig. 3, element 319a; Examiner's note: It would have been known at the time of invention that an interface is utilized to couple messages between busses]*; the pipeline units are each operable to analyze the message* [see Wong, Col. 10, lines 37-46; Examiner's note: Block configuration words are used to validate the message received, that is, to validate that the pipeline unit is the correct unit to receive the message.]*; the identified pipeline unit is operable to accept the message; and the other pipeline circuits are operable to reject the message* [see Wong, Col. 10, lines 7-10; lines 37-45; Examiner's note: Wong uses the function map table (Fig. 18a) to and the block configuration words (Fig. 18b) to correctly allow the corresponding pipeline unit to process the data and the other pipeline units to reject processing of the data.].

27. Regarding **claim 13,**

28. Wong discloses *the computing machine of claim 11, further comprising: wherein the communication bus comprises a plurality of branches.*[see Wong, Fig. 6, double-arrowed busses between communication bus 609 and elements 610a,b], *a respective branch* [see Wong, Fig. 6, double-arrowed

busses between communication bus 609 and elements 610a,b] *coupled to each pipeline unit* [see Wong, Fig. 6, element 610a,b]*; wherein the processor is operable to generate a message that identifies one of the pipeline units* [see Wong, Col. 9, lines 2-4 (instruction to turn control over to ACM); Col. 10, line 37 (a load instruction to specify which plane of DPUs to load)] *and to drive the message onto the pipeline bus* [Examiner's note: It is inherent with respect to Figure 3, that data is transferred between the CPU and ACM via a bus and bus interfaces]*; and a router coupled to each of the branches and to the pipeline-bus interface* [see Wong, Fig. 6, element 611a,b; Examiner's note: elements 611a/b determine the interconnect if any between DPUs (Col. 5, lines 26-28)] *and operable to receive the message from the pipeline-bus interface and to provide the message to the identified pipeline unit* [see Wong, Col. 5, lines 22-28; Examiner's note: Wong discloses the BLU receiving messages from the communication bus and thus the interface and configuring the datapath accordingly, thus providing the message.].

29. Regarding **claim 15**,

30. Wong discloses *a method, comprising: sending data to first of a plurality of pipeline units via a communication bus* [see Wong, Col. 9, lines 2-4; Examiner's note: Wong discloses sending data to the coprocessor registers, it would have been inherent that upon configuration, a hardwired pipeline would require a starting position for processing data.], *each pipeline unit including a respective hardwired pipeline* [see Wong, Fig. 6, element 621a et al. ("DPU" elements); Col. 5, lines 12-15 ("The DPUs provide the data path functionality for the behavioral mapping...")]*; and processing the data with the first pipeline unit* [see Wong, Col. 9, lines 4-7; Examiner's note: In this cite, Wong discloses an overall process, it is inherent that this overall process would contain processing of a first pipeline unit.].

31. Regarding **claim 16**,

32. Wong discloses *the method of claim 15 wherein sending the data comprises: sending the data to a router* [see Wong, Col. 5, lines 22-24; Examiner's note: Data is sent from the CPU to the BLU.]*; and providing the data to the first pipeline unit with the router via a respective first branch of the*

communication bus [see Wong, Col. 5, lines 26-28; Examiner's note: Bus 609 in Fig. 6 allows transfer of both control and data to BLU 610a. BLU 610a controls the configuration of DPUs in pipeline unit 620a and transfers data through the bus located between the BLU and DPUs as shown in Fig. 6].

33. Regarding **claim 17**,

34. Wong discloses *the method of claim 15 wherein sending the data comprises sending the data to the first pipeline unit with a processor* [see Wong, Col. 6, lines 2-4].

35. Regarding **claim 18**,

36. Wong discloses *the method of claim 15 wherein sending the data comprises sending the data to the first pipeline with a second of the plurality of pipeline units* [see Wong, Fig. 6, elements 630a; Col. 9, lines 47-50; Examiner's note: Wong discloses an inter-block communication bus (likened to buses connecting pipeline units in Fig. 8 of the applicant) that enables blocks to send data to each other. Given the multi-block function disclosed by Wong in Col. 9, it would have been obvious that a second unit could send data to a first unit via the inter-block bus.].

37. Regarding **claim 19**,

38. Wong discloses *the method of claim 15, further comprising driving the processed data onto the communication bus with the first pipeline unit* [see Wong, Col. 5, lines 24-26; Examiner's note: Bus 609 allows for bidirectional transfer of data from the ACM to the CPU. It would have been apparent that after data has finished processing it would have been steered back to the processor via Bus 609 (Col. 9, lines 4-7)].

39. Regarding **claim 20**,

40. Wong discloses *the method of claim 15 wherein processing the data with the first pipeline unit comprises: receiving the data from the communication bus with a hardwired-pipeline circuit* [see Wong, Fig. 6/7, element 609; Col. 5, lines 24-26], *loading the data into a memory with the hardwired-pipeline circuit* [see Wong, Col. 9, lines 2-4], *retrieving the data from the memory with the hardwired-pipeline*

circuit [see Wong, Col. 4, lines 55-57; Examiner's note: Wong discloses data passing from a register (within the ACM/LSM fabric) to a DPU ("cloud"), thus Wong discloses reading data from a memory coupled to a hardwire-pipeline circuit.], *and processing the retrieved data with the hardwired-pipeline circuit* [see Wong, Fig. 5, element 503].

41. Regarding **claim 21**,

42. Wong discloses *the method of claim 15 wherein processing the data with the first pipeline unit comprises: receiving the data from the communication bus with a hardwired-pipeline circuit* [see Wong, Fig. 6/7, element 609; Col. 5, lines 24-26], *processing the received data with the hardwired-pipeline circuit* [see Wong, Fig. 5, element 503], *and loading the processed data into a memory with the hardwired-pipeline circuit* [see Wong, Col. 9, lines 2-4], *and retrieving the processed data from the memory with the hardwired-pipeline circuit* [see Wong, Col. 4, lines 55-57; Examiner's note: Wong discloses data passing from a register (within the ACM/LSM fabric) to a DPU ("cloud"), thus Wong discloses reading data from a memory coupled to a hardwire-pipeline circuit.], *and driving the processed data onto the communication bus with the hardwired-pipeline circuit* [see Wong, Col. 9, lines 4-7; Examiner's note: Wong discloses results being sent back to the main processor, which would have utilized the communication bus].

43. Regarding **claim 22**,

44. Wong discloses *the method of clam 15, further comprising: generating a message that includes the data and that identifies the first pipeline unit as a recipient of the message* [see Wong, Col. 9, line 45; Examiner's note: Wong discloses a load instruction which specifies which block a function is to reside in.]; *and wherein sending the data to the first pipeline unit comprises determining from the message that the first pipeline is a recipient of the message* [see Wong, Col. 10, lines 7-10; lines 37-45; Examiner's note: Wong uses the function map table (Fig. 18a) to and the block configuration words (Fig. 18b) to

correctly allow the corresponding pipeline unit to process the data and the other pipeline units to reject processing of the data.].

Claim Rejections - 35 USC § 103

45. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

46. Claims 4, 8, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong.

47. Regarding **claim 4**,

48. Wong discloses the limitations as stated in **independent claim 1**

49. Wong does not explicitly disclose *each of the hardwired-pipeline circuits is disposed on a respective field-programmable gate array.*

50. However, Wong does disclose the hardwired-pipeline circuits being disposed on a reconfigurable "course-grained silicon implementation" (Col. 5, line 36). Furthermore, Wong discloses the use of FPGAs for the same utility (Col. 5, line 37) and furthermore discloses the disadvantages of utilizing an FPGA (Col. 5, lines 37-38). Furthermore, Wong discloses the point that FPGA implementations are more flexible (Col. 1, lines 51-52) and were not used within the invention due to the preferred nature of courser-grained silicon for long bit width arithmetic function modules (Col. 5, lines 39-40). The advantage, disclosed by Wong, of utilizing FPGAs for a hardwired-pipeline circuit would therefore have been to include a higher level of flexibility. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize an FPGA as a hardwired-pipeline circuit in place of the

courser-grained silicon if a higher degree of flexibility was needed without heed to long bit arithmetic function modules.

51. Regarding **claim 8**,

52. Wong discloses the limitations as stated in **independent claim 1**.

53. Wong also discloses *the communication bus* [comprising] *a plurality of branches* [see Wong, Fig. 6, double-arrowed busses between communication bus **609** and elements **610a,b**], *a respective branch coupled to each pipeline unit; a router coupled to each of the branches* [see Wong, Fig. 6, coupling of double sided arrow to 610a/620a]; *a pipeline bus* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24; Examiner's note: It would have been obvious to one of ordinary skill in the art at the time of invention that the bus interfaces would have been coupled to the CPU and to a corresponding datapath slice.]; *a pipeline-bus interface coupled to the router and to the pipeline bus* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24].

54. Wong does not explicitly disclose *a secondary bus coupled to the router.*

55. However, Wong does disclose the use of a MAC controller (Fig. 3, element 304), which is commonly used to access a network. However, Wong does not explicitly disclose how the MAC controller interfaces with the ACM within the disclosure. Given the state of the art at the time of invention, it would have been known that vector processors are well suited for handling large quantities of raw data and a mechanism for routing data directly to the pipeline units would have been advantageous. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to assume that the MAC controller disclosed by Wong would have been coupled to the router disclosed by Wong with the intention of facilitating the transmission of raw data for processing.

56. Regarding **claim 14**,

57. Wong discloses the limitations as stated in **independent claim 11**.

58. Wong also discloses *the communication bus* [comprising] *a plurality of branches* [see Wong, Fig. 6, double-arrowed busses between communication bus **609** and elements **610a,b**], *a respective branch coupled to each pipeline unit* [see Wong, Fig. 6, coupling of double sided arrow to 610a/620a]; *and a router coupled to each of the branches* [see Wong, Fig. 6, element 611a,b; Examiner's note: elements 611a/b determine the interconnect if any between DPUs (Col. 5, lines 26-28) thus routing functions to individual pipeline units.] [and] *to the pipeline bus interface* [see Wong, Fig. 3, elements 319a,b].

59. Wong does not explicitly disclose *a secondary bus and a router coupled to the secondary bus.*

60. However, Wong does disclose the use of a MAC controller (Fig. 3, element 304), which is commonly used to access a network. However, Wong does not explicitly disclose how the MAC controller interfaces with the ACM within the disclosure. Given the state of the art at the time of invention, it would have been known that vector processors are well suited for handling large quantities of raw data and a mechanism for routing data directly to the pipeline units would have been advantageous. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to assume that the MAC controller disclosed by Wong would have been coupled to the router disclosed by Wong with the intention of facilitating the transmission of raw data for processing.

Conclusion

61. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Pat. No. 6,112,288 to Ullner discloses an application specific pipeline accelerator chip.

US Pat. Appl. Pub. 2002/0087829 to Snyder et al. discloses a set of parallel processors coupled to a controller and system bus.

US Pat. No. 4,873,626 to Gifford discloses a parallel processing array coupled to a group bus interface.

US Pat. No. 6,023,742 to Ebeling et al. discloses a reconfigurable parallel system of pipelines and control mechanisms.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Zalepa whose telephone number is (571) 272-6754. The examiner can normally be reached on Monday-Friday (alt. Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GDZ

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